

A 60GHz MMIC Chipset for 1-Gbit/s Wireless Links

Kohei Fujii, Miroslaw Adamski, Piero Bianco, Daniel Gunyan, John Hall, Ron Kishimura, Camille Lesko, Matthias Schefer, Steve Hessel, Henrik Morkner, and Antoni Niedzwiecki
Agilent Technologies, Inc.

Abstract - This paper describes the development of a MMIC chipset for 60GHz radio links and radars. The chipset includes a low noise amplifier, an image rejection mixer, a frequency quadrupler, and a power amplifier. All were optimized to work together as a 1-Gbit/s radio link in the unlicensed 59GHz to 64GHz wireless band, although most are suitable for any application from 55GHz to 70GHz. These MMICs are fabricated in Agilent's advanced e-beam PHEMT process and have been demonstrated in fully operational 1-Gbit/s radio-links in field testing.

I. Introduction

Occasionally fiber optic links must be switched to wireless due to economic, environmental, or logistic reasons. Figure 1 shows a general system structure for a 1-Gbit/s radio-link. The radio is a self contained unit which converts a fiber optic input to 60GHz transmit and receive. The radios have the frequency band structure shown in Figure 2. Units are used in pairs of Low Band Tx and High Band Tx units. A single Select Channel (SC) command (on the RS232 port) selects the channel for both transmitter and receiver.

The 60GHz unlicensed frequency band is ideal for wireless short haul links up to 1 km due to its directivity and wide bandwidth. A 1-Gbit/s data stream can be processed and up-converted to this band, then transmitted, received, and down-converted. One of the prime challenges is the availability of economic, reliable, high performance MMICs that operate at these frequencies. This paper describes four such MMICs designed and built by Agilent Technologies for sale and usage in 60GHz radio links.

II. Millimeter-Wave Process and CAD tools

Agilent's mm-wave PHEMT process [1] uses an e-beam $0.125\mu\text{m}$ gate. The device has a f_T of 90GHz. The wafer material is selected for high power and breakdown with some compromises for noise. A Ti/Pt/Au T-gate is used for low input resistance and

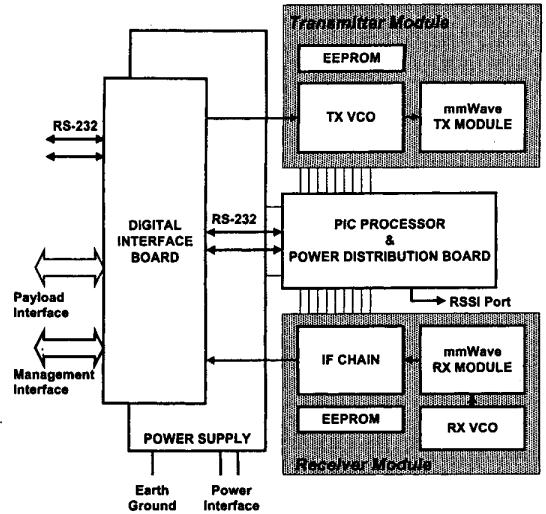


Figure 1. One gigabit link architecture using a 60 GHz MMIC chipset

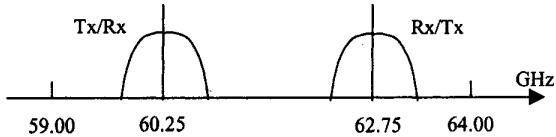


Figure 2. Frequency bands used by radio link

high reliability. The process is designed to operate with a peak drain voltage up to 5.5V. The $0.125\mu\text{m}$ PHEMT device delivers a 1dB-gain compression output power of 120mW/mm and a saturated power of 210mW/mm at 65GHz. All steps (except gate) are defined using stepper lithography on 3-inch wafers.

The MMIC process is equipped with passive components which include a $200\Omega/\square$ n-layer bulk resistor, $22\Omega/\square$ Ta_2N thin film resistor, $0.58\text{fF}/\mu\text{m}^2$ Si_3N_4 MIM capacitor, 23pH backside via and two metal layers for transmission lines.

The process includes 100% on wafer MMIC test and verification of performance. Agilent ADS with complete Root models [2-3] is used for simulation and performance measurement. Agilent Momentum is used for passive structures.

III. MMIC Chipset & Results

Low Noise Amplifier

A designed and fabricated LNA consisted of 60 μ m, 120 μ m, and 168 μ m FETs. A three-stage amplifier configuration is used to achieve more than 14dB gain at 60GHz. For matching, shorted microstrip transmission line stubs were used to minimize the chip size. Figure 3 shows a photograph of the LNA. The circuit utilized a stabilizing topology in the drain and gate bias to provide unconditional stability. The measured performance is shown in Figure 4. The LNA has more than 14dB gain with 5dB noise-figure at 60GHz. Two LNA MMICs are typically cascaded in the system to achieve more than 28dB small-signal gain.

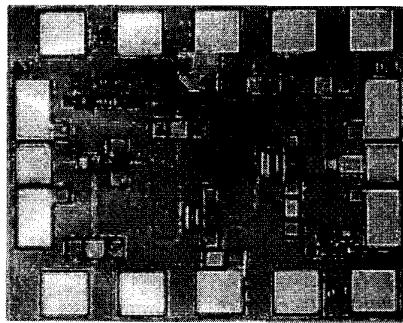


Figure 3. Photograph of the LNA. (950 x 800 μ m)

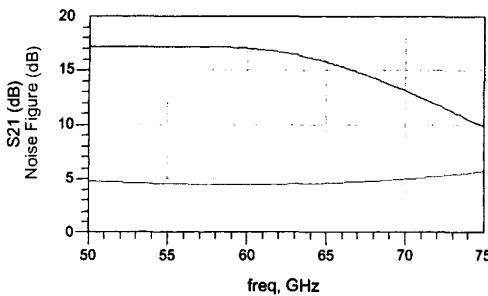
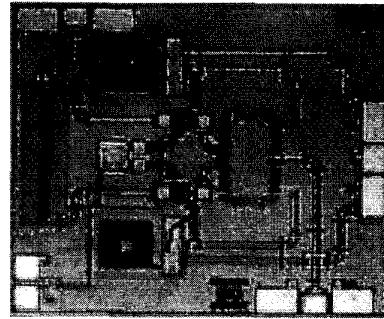


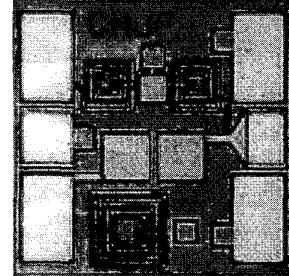
Figure 4. Measured performance for the LNA. The biasing condition is $V_{ds} = 1.5V$, $V_{gs} = -0.3V$.

Image Rejection Mixer

Most conventional mixers use filters to attenuate the image, or they suffer a 3dB noise figure increase. For this application an image rejection mixer (IRM) is one of the best solutions. Filtering could be used, but for a 60GHz link, the image frequency is close to the local oscillator frequency and hard to suppress. The designed and fabricated IRM consists of two MMIC chips: a mixer and a 90-degree IF hybrid. The mixer MMICs are shown in Figure 5 (a) and (b) respectively. The mixer MMIC consists of a pair of 75 μ m PHEMTs, Lange coupler, Wilkinson power divider, and matching circuits. The mixer employs a drain-pumped passive mixer [4] to maximize the conversion gain and the local pumping power. The 90-degree IF hybrid consists of high pass and low pass filters, [5] and those filters are realized by lumped-passive components. The IF hybrid has less than 1dB total power loss and less than 10-degrees phase error between 2GHz and 5GHz IF bandwidth. Figure 6 shows the measured mixer performance. The tested mixer has less than -10dB conversion gain and more than 19dB image rejection ratio between 50GHz and 69GHz.



(a) Mixer MMIC. (1400 x 1100 μ m)



(b) 90-degree IF hybrid MMIC. (470 x 470 μ m)

Figure 5. Photographs of the image rejection mixer

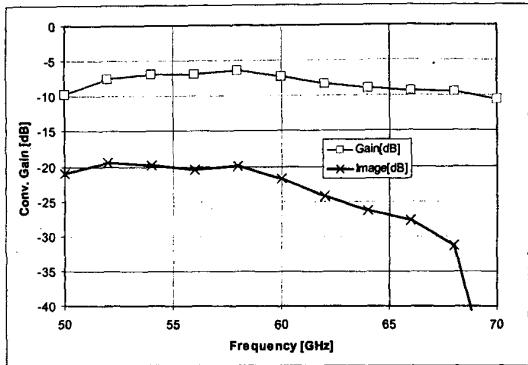


Figure 6. Measured performance for the mixer. The biasing condition is $V_{ds} = 0V$, $V_{gs} = -0.4V$, and the IF frequency is 2.5GHz with 6dBm local pumping power.

Frequency Quadrupler

A frequency quadrupler permits the use of 15GHz oscillators in 60GHz applications. Figure 7 shows a photograph of the designed and fabricated frequency quadrupler.

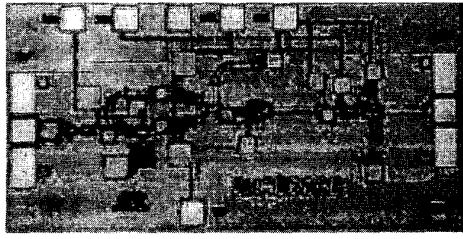


Figure 7. Photograph of the frequency quadrupler. (1200 x 800 μm)

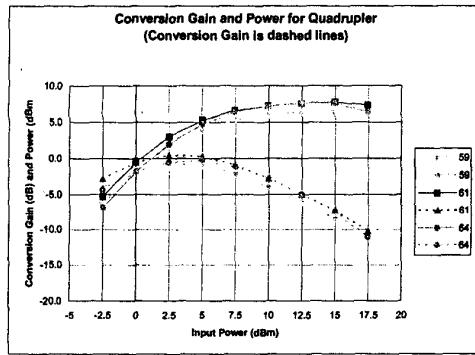


Figure 8. Measured performance of the frequency quadrupler

The quadrupler consists of a balanced doubler stage to reject the fundamental frequency. An active balun is employed to realize a balanced frequency doubler. This is followed by another doubler stage and a high-pass filter to reject the second and third harmonics (30GHz and 45GHz).

Measured performance is shown in Figure 8. The measured quadrupler has a conversion gain of -2.5dB for a 7dBm, 60GHz output frequency. The temperature coefficient for Psat is -0.06 dB/deg C.

Power Amplifier

Figure 9 shows a photograph of the power amplifier. The power amplifier has a four-stage configuration with 60 μm , 70 μm , 140 μm , and 300 μm PHEMTs. The amplifier employs a reactive matching technique to maximize frequency bandwidth and frequency flatness. The amplifier also employs stabilizing resistors in the gate and drain biasing circuits. Figure 10 shows the measured small-signal performance. The amplifier has more than 20dB small-signal gain between 38GHz and 70GHz. The 1dB compression point is more than 14dBm.

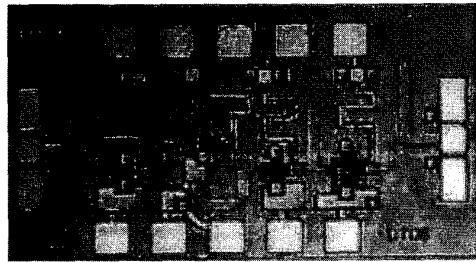


Figure 9. Photograph of the power amplifier (1200 x 800 μm)

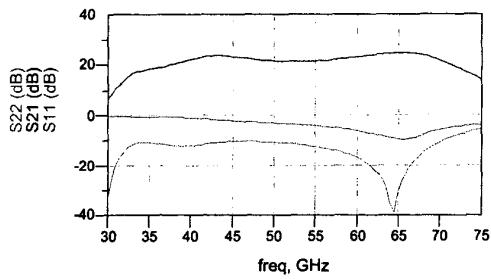


Figure 10. Measured performance of the power amplifier

IV. Radio-link Application Example

The MMIC chipset was assembled in a 60GHz radio-link system shown in Figure 1. Block diagrams for mm-wave modules are shown in Figure 11. Filters, couplers and transmission lines are fabricated using coplanar waveguide on 10mil alumina thin-film substrates. MMIC chips are eutectically mounted onto the thin-film substrates. Since the MMIC chipset employs an optimized RF bonding pad structure, an industry standard 1mil wire-bonding technique was applied for the RF signaling and DC biasing. This technique drastically reduces assembly cost, and realizes high volume manufacturing possibilities for mm-wave modules.

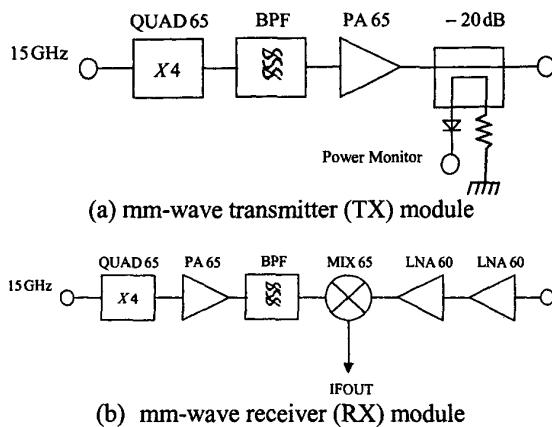


Figure 11. Block diagram for transmitter and receiver modules

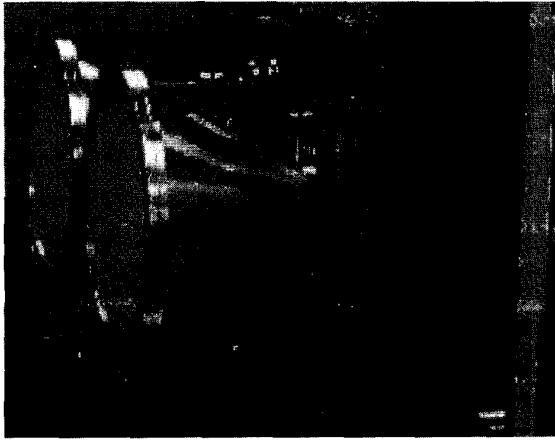


Figure 12. A photograph for the 60GHz radio

A complete 60GHz radio-link system shown in Figure 12 has been field tested at an 80m-range. The

tests were done with the Agilent bit error rate tester (BERT) and Internet Advisor. With the BERT, we measured BER=1e-12 and 13dB power margin, which translates to 250m maximum distance (data rate 1250Mb/s). The test patterns were K28.5, pseudo random bit sequence (PRBS) $2^7 - 1$, and a several thousand bit long Gigabit Ethernet pattern. The Internet Advisor showed full throughput up to a BER of 1e-9. This test was in simplex mode.

V. Conclusion

We have described the design and performance of a MMIC chipset for 60GHz radio links. The MMICs are also suitable for radar and other applications in the 50GHz to 70GHz ranges. A 1-Gbit/s radio link system has employed these MMICs and has been shown fully functional to 1-Gbit/s data rate with BER=1e-12.

The MMICs shown were a LNA, a mixer, a frequency quadrupler, and a power amplifier. All were fabricated in Agilent's 0.125μm PHEMT technology, well capable of reliable volume production. Photographs, descriptions, and measured results have been shown. To our knowledge this is the only integrated chipset capable of such 60GHz performance on a production scale.

Acknowledgements

The authors wish to thank the large team that worked on this chipset. Many individuals including Betty Szeto, Jay Coward, and Lan Ton were involved to make this a reality.

References

- [1] Hiroshi Kondo, et al., "A manufacturable 50GHz MMIC process and circuit applications," IEICE Technical report, vol. 92, no. 417, ED92-137, pp.43-48, 1993.
- [2] D.E. Root, "Measurement-based mathematical active device modeling for high frequency circuit simulation," IEICE Trans. Electron., vol. E82-C, no. 6, pp. 924-936, June 1999.
- [3] John Wood, and D.E. Root, "Bias-dependent linear scalable millimeter-wave FET model," IEEE Trans. On MTT, vol. 48, no. 12, pp. 2352-2360, December 2000.
- [4] Ron Reeves, and Vern Brady, "Monolithic Ka-Band FET receiver chips," 1994 IEEE MTT-S Digest, pp. 119-121, 1994.
- [5] Lawrence Larsen, "RF and Microwave circuit design for wireless communications", Artech House, 1996, pg. 254.